Ms. Manu Bansal

Designation: Assistant Professor

Specialization:

VLSI Design, Cryptography and Steganography, Digital Signal Processing

Email: mbansal@thapar.edu

Contact No.: 9417162059

Education:

- Ph.D. (Submitted May, 2018) Topic –"Study and Analysis of Minimization Algorithms for VLSI Circuit Synthesis" under the supervision of Dr. Alpana Agarwal, TIET Patiala.
- M.E. (Electronics & Communication), TIET, Patiala
- B.E. (Electronics & Communication), TIET, Patiala

Experience: 20 years

- Thapar Institute of Engineering & Technology, Patiala Since Feb 27, 1998.

Sponsored Research Projects:

- SMDP Chips to System Design, MeitY sponsored, **Rs. 166 Lakhs** , (**Consortium Budget 99.97 Crores**) 2 015 - 2020. **(Co-Chief Investigator) Ongoing**
- Special Man power Development Program for VLSI Design and Related Software (Phase – I), **DOE sponsored, Rs. 75 Lakhs , 1998 – 2005. (Team Member)**

Major Publications:

- Kumar, N., Bansal, M. and Kumar, N., 2012. VLSI Architecture of Pipelined Booth Wallace MAC Unit. International Journal of Computer Application (0975-8887).

- Rehan, Sanisha and Bansal, Manu, 2013. Performance comparison among different evolutionary algorithms in terms of node count reduction in BDDs. International Journal of VLSI and Embedded Systems, 4, pp.1-6.
- Pathak, K. and Bansal, M., 2017. A FPGA based Steganographic System Implementing a Modern Steganalysis Resistant LSB Algorithm. Defence Science Journal, 67(5), p.551.
- Manu Bansal, Alpana Agarwal, “Low Power Optimization Technique and a genetic minimization algorithm for variable ordering of BDD mapped VLSI Circuits” International Journal of Electrical & Computer Sciences IJECS-IJENS Vol:17 No:05 1 163605-8282-IJECS-IJENS © October 2017.
- Manu Bansal, Alpana Agarwal, “ A Genetic Algorithm for ordering and reduction of BDDs using Crossover Operators for MIMO VLSI Circuits” Research Cell: An International Journal of Engineering Sciences, Issue July 2017, Vol. 24,pp123-129.

International Conferences

- Bansal, M. and Agarwal, A., 2013, September. Ordering and reduction of BDDs for multi-input adders using evolutionary algorithm. In Advanced Electronic Systems (ICAES), 2013 International Conference on (pp. 127-130). IEEE.
- Manu Bansal and Alpana Agarwal , Genetic Algorithm for Ordering and Reduction of B DDs for MIMO Circuits, The Third International Conference on Innovative Computing Technology London, UK, August 29 - 31, 2013

Thesis Guided

- Guided 50 ME/M.Tech thesis

Foreign Visits

- Visited London for conference presentations

Short Term Courses/Workshops/Conferences Organized: 5

Short Term Courses/Workshops/Conferences Attended: More than 20

Membership of Professional Organizations

- Life Member, Indian Society of Systems Electronics and Telecommunication Engineers (IETE)
- Life Member, Metrology Society of India (MSI)

- Member, VLSI Society of India (VSI)

Major Administrative Responsibilities

- UG BE ECE Incharge 2014 onwards
- Laboratory Incharge, Digital electronics Lab, (2005 – 2008)
- Laboratory Incharge, VLSI Chips to Systems (2015 – present)
- Member, DPPC (2014 – Present)
- Member, DAAC , BOS of ECED (Several occasions, Present)
- Member, DAAC BE(Mechatronics) (2012 - Present)
- Departmental Student Counselor (1997 – 2002).
- Member of Senate for 1997, 2000, 2004, 2007, 2008 - 09, 2017.
- Departmental ISO Co-odinator since 1998 till 2017.
- Departmental Souvenir Co-odinator from 2013 till 2017
- NSS Co-odinator of two wings from 2012 to 2016.
- Internship Co-odinator 2014 onwards.