### PROPOSED SCHEME OF COURSES FOR M. Tech. (VLSI Design) 2017 - 2019

#### First Semester

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<td>1.</td>
<td>PVL108</td>
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**Total Credits – 76.0**
## List of Electives

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PVL108: Device Physics and Technology

Course Objectives: To understand the physics of semiconductor, basic theory of Metal Semiconductor Contacts and PN junction, construction and operation of BJT and MOSFET and basic theory, operation and structure of MOS transistors, basic theory of Crystal Growth and Wafer Preparation, Epitaxy, Diffusion and Ion-implantation, Oxidation, Lithography, Etching and Nano-Fabrication.


Semiconductor Devices: p-n Junction, Thermal Equilibrium Condition, Depletion Region and Capacitance, IV and CV characteristics, Charge storage, Transient Behaviour, Junction Breakdown, Metal Semiconductor Contacts, Tunnel diode- applications of tunnelling, Photonic Devices-LEDs, Semiconductor Laser, Photodiode, Bipolar Transistor - Static Characteristics, Frequency Response and Switching, Thyristor, MOSFET Fundamentals and Scaling, MESFET, CMOS.


Course Learning Outcomes:
The students are able to:

1. Understand the basic physics of semiconductor devices and the basics theory of PN junction.
2. Understand the basic theory of MOS transistors.
3. Understand the basic steps of fabrication.
4. Learn the basics theory of Crystal Growth and Wafer Preparation.
5. Study the Epitaxy, Diffusion, Oxidation, Lithography and Etching.
6. Understand the basic theory of Nano-Fabrication.

References:


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Course Objectives: In this course the students will learn logic synthesis with design optimization techniques, VHDL and SystemC design concepts, Combinational logic concepts, sequential VHDL processing and FPGA.

Introduction: Concepts of Hardware Description Languages and logic synthesis.

Logic synthesis: Design cycle, types of synthesizers, design testing and verification, design optimization techniques, technology mapping, VHDL design hierarchy, objects, types and subtypes, design organization, VHDL design cycle.

Combinational Logic: Design units, entities and architectures, simulation and synthesis model, signals and ports, simple signal assignments, conditional signal assignments, selected signal assignment.

Types and Operators: Synthesizable types, standard types, standard operators, scalar types, records, arrays, attributes, standard operators, operator precedence, Boolean operators, comparison operators, arithmetic operators, concatenation operators.

Package std_logic_arith: std_logic_arith package, making the package visible, content s of std_logic_arith, resize functions, operators, shift functions, type conversions, constant values, mixing types in expressions, numeric packages.

Sequential VHDL: Processes, signal assignments, variables, if statements, case statements.

Registers: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers, simulation model of asynchronous reset, asynchronous reset templates, registered variables.

Hierarchy: Role of components, using components, component instances, component declaration, Configuration specifications, default binding, binding process, component packages, generate statements.

Sub programs: Functions, type conversions, procedures, declaring subprograms.

Test Benches: Test benches, verifying responses, printing response values, reading data files.

FSM: Moore and Mealy machine modelling

FPGA: Introduction, Logic Block Architecture, Routing Architecture, Programmable, Interconnection, Design Flow, Xilinx Virtex-II (Architecture), Boundary Scan, Programming FPGA's,

SystemC:
Overview: Capabilities, Design Hierarchy, Data Types, Modelling combinational Logic, Modelling Sequential Logic, Writing Testbenches
Laboratory Work: Modelling and simulation of all VHDL and SystemC constructs using Model Sim, their testing by modelling and simulating test benches, Logic Synthesis using FPGA Advantage, Mapping on FPGA Boards.
**Course learning outcome (CLO):** The student will be able to

1. Model digital systems in VHDL and SystemC at different levels of abstraction.
2. Partition a digital system into different subsystems.
3. Simulate and verify a design.
4. Transfer a design from a version possible to simulate to a version possible to synthesize.
5. Use computer-aided design tools to synthesize, map, place, routing, and download the digital designs on the FPGA board.

**Text Books:**


**Reference Books:**


**Evaluation Scheme:**

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Course Objectives: To understand the physics and modeling of MOSFETs, basic theory of fabrication steps and layout of CMOS Integrated Circuits, basic theory of Power Dissipation in CMOS Digital Circuits and Foster ability to work with static and dynamic logic circuits.


Static CMOS Logic Elements: Complex Logic Functions, CMOS NAND Gate, CMOS NOR Gate, Complex Logic Gates, Exclusive OR and Equivalence Gates, Adder Circuits, Pseudo nMOS Logic Gates, Schmitt Trigger Circuits, SR and D-type Latch, CMOS SRAM Cell, Tri-state Output Circuits.


Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families: Charge Leakage, charge Sharing, Dynamic RAM Cell, Bootstrapping, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Multiple-Output Domino Logic, NORA Logic, Single-Phase Logic.


CMOS Differential Logic Styles: Dual-Rail Logic, CVSL, CPL, DPL, DCVS, MCML.

Laboratory work: Familiarization with schematic and layout entry using Mentor/ Cadence/ Tanner Tools, circuit simulation using SPICE; DC transfer Characteristics of Inverters, Transient response, Calculating propagation delays, rise and fall times, Circuit design of inverters, complex gates with given constraints; Circuit Simulation and Performance Estimation using SPICE; Layouts of Inverters and Complex gates, Layout Optimization, Design Rule Check (DRC), Electrical Rule Check (ERC), Comparison of Layout Vs. Schematics, Circuit Extraction.

Course Learning Outcomes:
The students are able to:
1. Understand the basic Physics and Modeling of MOSFETs.
2. Learn the basics of Fabrication and Layout of CMOS Integrated Circuits.
3. Study and analyze the performance of CMOS Inverter circuits on the basis of their operation and working.
4. Study the Static CMOS Logic Elements.
5. Study the Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families.

Recommended Books:

Evaluation Scheme:

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PVL110 : VLSI Architectures

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Course objective: The motive of this course is to inculcate the knowledge of the different processors; their architecture and organizational intricacies. For performance enhancement consideration is given to various instruction level and memory management techniques such as pipelining, parallelism, instruction scheduling, hierarchical memory management etc. Study of the superscaler architecture organization, design issues and Power PCs is to be carried out.

Introduction: Review of basic computer architecture, quantitative techniques in computer design, measuring and reporting performance. CISC and RISC processors. Processor organization and Architectural Overview.

Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards, and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques, dynamic instruction scheduling

Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.

Instruction-level parallelism: basic concepts, techniques for increasing ILP, superscalar, super-pipelined and VLIW processor architectures. Array and vector processors.


Course Learning Outcome (CLO):
The students will able to:
1. To review the basics of different processors including architecture and organization
2. To foster ability of handling and designing different types of pipelining techniques; exception handling corresponding instruction scheduling.
3. To understand various memory organization and management techniques
4. To understand the various advanced architectures.
5. To achieve the understanding of parallel, shared architectures and important organizational details of superscaler architecture

Text Books:

Reference Books:

Evaluation Scheme:

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Course Objectives: To introduce analog MOS processes layout techniques, single stage amplifiers, working of differential amplifiers with frequency response, and noise impact.


Single Stage Amplifiers: Common Source Stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode.

Differential Amplifier: Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell.

Current Sources and Mirrors: Current Sources, Basic Current Mirrors, Cascode Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis.

Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.

Voltage References: Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References.

Feedback: General Considerations, Topologies, Effect of Loading.

Operational Amplifier: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR.

Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques.

Noise: Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

Switched-Capacitor Circuits: Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

Laboratory work: Review of Mentor Tools; Analysis of Various Analog Building Blocks such as, Current and Voltage References/Sources, Current Mirrors, Differential Amplifier, Output Stages; Design and Analysis of Op-Amp (Closed loop and open loop) and its Characterization, Switched-Capacitor Integrator; Analog Layout Constraints, Layout Designs and Analysis.

Course Learning Outcomes:
The student will be able to:
1. Apply knowledge of mathematics, science, and engineering to design and analysis of analog integrated circuits.
2. Identify, formulates, and solves engineering problems in the area of analog integrated circuits.
3. Use the techniques, skills, and modern programming tools such as Mentor Graphics, necessary for engineering practice.
4. Participate and function within multi-disciplinary teams.

Recommended Books:

Evaluation Scheme:

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Course objective: To understand the causes of the power dissipation in digital ICs, quantitative analysis of power dissipation in VLSI circuits and exploring the low power circuits and architectures for VLSI system.

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Sources of Power Dissipation: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design: Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library, logic level, Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Leakage Power Minimization Approaches: Variable threshold voltage CMOS (VTCMOS) approach. Multi-threshold-voltage CMOS (MTCMOS), Dual-Vt assignment approach (DTCMOS), Transistor stacking.

Low Power Static RAM Architecture: Architecture of SRAM array, Reduced Voltage Swings on Bit Lines, Reducing power in memory peripheral circuits

Text/References:


Course Learning Outcomes:
The student will be able to:
    1. Understand the need for low power in VLSI.
2. Understand various dissipation types in CMOS.
3. Estimate and analyse the power dissipation in VLSI circuits.
4. Understand the probabilistic power techniques.
5. Derive the architecture of low power SRAM circuit.

**Evaluation Scheme:**

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Course Objective: In this course students will learn test economics, fault modelling, logic and fault simulation, ATPG concepts for combinational and sequential circuits. Students will also able to write testbench for the complex VLSI design using System Verilog.

Introduction: Role of testing in VLSI design, Issues in test and verification of complex chips, VLSI test process and equipment, Test economics, Yield analysis and product quality.

Faults modelling and fault simulation: Physical faults and their modelling, Stuck-at faults, Bridging faults, Fault collapsing, Fault simulation, Deductive, Parallel and Concurrent fault simulation, Combinational and sequential SCOAP measures.

ATPG for combinational circuits: D-Algorithm, Boolean Difference, PODEM, Random, Exhaustive and Weighted Test Pattern Generation, Aliasing and its effect on Fault coverage.

ATPG for sequential circuits: ATPG for Single-Clock Synchronous Circuits, Time frame expansion method, Simulation-Based Sequential Circuit ATPG.

Memory testing and BIST: Permanent, Intermittent and pattern sensitive faults, March test notion, Memory testing using march tests, PLA testing, Ad-Hoc DFT methods, Scan design, Partial scan design, Random logic for BIST, Memory BIST.

Verification: Design verification techniques based on simulation, Analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Hardware verification language: Introduction to System Verilog, Development of stimulus generator, Monitor and complete test bench using System Verilog.

Laboratory Work:
Familiarization with development of testbenches using Verilog/SystemVerilog on Mentor/Cadence/Xilinx-ISE tools, Logic simulation, Logic level diagnosis, ATPG, development of verification plan for the given design and writing testcases, computation of fault-coverage/code-coverage index.

Text Books:

Reference Books:
Course Learning Outcomes:
The student will be able to

1. Acquire knowledge about fault modeling and collapsing.
2. Learn about various combinational automatic test pattern generation techniques.
3. Learn about various sequential automatic test pattern generation techniques.
4. Analyze different memory faults and its testing methods.
5. Develop the verification plan for the small to complex VLSI designs.
6. Develop testbench using HVL for testing and verification of VLSI designs.

PVL203 VLSI SIGNAL PROCESSING

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Course objective: To know how to design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications. Explore optimization techniques indispensable in modern VLSI signal processing. immediate access to state-of-the-art, proven techniques for designers of DSP applications-in wired, wireless, or multimedia communications.


Algorithmic Transformations: Retiming, Cut-set retiming, Feed-Forward and Feed-Backward, Clock period minimization, register minimization, Unfolding, Sample period reduction, Parallel processing,
Bit-serial, Digit-serial and Parallel Architectures of DSP Systems, Folding, Folding order, Folding Factor, Folding Bi-quad filters, Retiming for folding, Register Minimization technique, Forward Backward Register Allocation technique.

**Systolic Architecture Design and Fast Convolution:** Systolic architecture design methodology, Projection vector, Processor Space vector, Scheduling vector, Hardware Utilization efficiency, Edge mapping, Design examples of systolic architectures, Cook-Toom Algorithm and Modified Cook-Toom Algorithm, Wniograd Algorithm and Modified Winograd Algorithm, Iterated Convolution, Cyclic Convolution.


**Course learning outcome (CLO):**

1. To learn performance optimization techniques in VLSI signal processing,
2. Transformations for high speed and power reduction using pipelining, retiming, parallel processing techniques, supply voltage reduction as well as for strength or capacitance reduction,
3. Area reduction using folding techniques, Strategies for arithmetic implementation,
4. Synchronous, wave, and asynchronous pipelining.

**Text Books:**


**Reference Books:**

**Evaluation Scheme:**

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<td>Sessionals (Assignments+Quizes)</td>
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Course Objectives: In this course the students will learn overview of nanoelectronic and nano devices, its mechanics and technologies, nano fabrication and characterization and its future aspects.

Shrink-down approaches: Introduction to Nanoscale Systems, Length energy and time scales, Top down approach to Nanolithography, CMOS Scaling, Limits to Scaling, System Integration Limits – Interconnect issues, etc.

Overview of Nanoelectronics and Devices: The Nano-scale MOSFET, FinFETs, Vertical MOSFETs, Resonant Tunneling Transistors, Single Electron Transistors, New Storage devices, Optoelectronic and Spin electronics Devices.

Basics of Quantum Mechanics: History of Quantum Mechanics, Schrödinger Equation, Quantum confinement of electrons in semiconductor nano structures, 2D confinement (Quantum Wells), Density of States, Ballistic Electron Transport, Coulomb Blockade, NEGF Formalism, Scattering.


Future Aspects of Nanoelectronics: Molecular Electronics: Molecular Semiconductors and Metals, Electronic conduction in molecules, Molecular Logic Gates, Quantum point contacts, Quantum dots and Bottom up approach, Carbon Nano-tube and its applications, Quantum Computation and DNA Computation, Overview of Organic Electronics: OLEDs, OLETs, Organic Solar Cells

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about nanoelectronics and shrink down approach.
2. Understand concept behind nanomosfets and nano devices.
3. Set up and solve the Schrodinger equation for different types of potentials in one dimension as well as in 2 or 3 dimensions for specific cases.
4. Understand the nanofabrication and characterization facilities.

Recommended Books:

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Course Objectives: In this course the students will learn interconnect models, device models, interconnect analysis and interconnect materials.


Device Models: Introduction, device I-V characteristics, General format of device Models, device models in explicit expression, device model using a table-Lookup model and effective capacitive model.


Crosstalk analysis: Introduction, Capacitive coupled and inductive coupled interconnect model and analysis, Transmission line based model.

Advanced Interconnect materials: Basic materials: Copper and aluminium. Problem with existing material in deep submicron: Electro-migration effect, surface and grain boundary effect. CNT as an interconnect, impedance parameters of CNT, types of CNT, GNR and Optical interconnects.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about Technology trends, Device and interconnect scaling.
2. Identify basic device and Interconnect Models.
3. Perform RLC based Interconnect analysis.
4. Understand the Problem with existing material in deep submicron.
5. Understand the advanced interconnect materials

Recommended Books:

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Course Objectives: In this course the students will learn data processing elements with various architecture design, PLA design concepts, memory design with its clock issues.


Design of Control Part: Moore and Mealy Machines, PLA Based Implementation, Random Logic Implementation, Micro-programmed Implementation.


Memory Design: SRAM cell, Various DRAM cells, RAM Architectures, Address Decoding, Read/Write Circuitry, Sense Amplifier and their Design, ROM Design.

Clocking Issues: Clocking Strategies, Clock Skew, Clock Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree. Synchronization Failure and Meta-stability.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge to Design of Data Processing Elements.
2. Design of Control Part of digital logic circuit.
3. Acquire knowledge about Structuring of Logic Design.
4. Identify Clocking Issues in digital system design

Recommended Books:

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Course Objectives: In this course the students will learn fundamental of semiconductor physics, quantum mechanics, carrier transport, MOSFET modelling and its analysis.

Semiconductor Fundamentals: Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations (electron statistics, density of states, effective mass, band gap narrowing, Review of PN and MS diodes.

Quantum Mechanics Fundamentals: Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling.

Modeling and Simulation of Carrier Transport: Carrier Scattering (impurity, phonon, carrier-carrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion.

MOS Capacitors: Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown).

MOSFET Modeling: Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices.


Advanced Device Technology: SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash). Sub-micron and Deep sub-micron Device Modeling.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about physics involved in modelling of semiconductor device.
2. Acquire the basic knowledge about quantum mechanical fundamentals.
4. Identify characteristics of Advanced Device Technology

Recommended Books:

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Course objectives: In this course the students will learn basics of optical fiber communication, optical waveguides, light sources, amplifiers, modulators, detectors, optical MEMS & NEMS and silicon photonics.

Introduction to Optical Fiber Communication: Nature of light; optical communication; optical fibers; propagation of light in optical fibers; transmission characteristics of optical fibers; fabrication of optical fibers.


Semiconductor Light Sources and Amplifiers: Spontaneous and stimulated emission, emission from semiconductors, semiconductor injection lasers, single frequency lasers, Various laser configurations, injection laser characteristics, VCSEL, LEDs - Introduction, LED power efficiency, LED structures, LED characteristics and Organic LEDs, Optical amplifiers, Semiconductor optical amplifier.


Optical Detectors: Optical detection principle, quantum efficiency and responsivity, semiconductor photodiodes with/without internal gain, Solar cell.

Optical MEMS and NEMS: Micro-electro-mechanical and nano-electro-mechanical systems, MEMS integrated tunable photonic devices-filters, lasers, hollow waveguides; NEMS tunable devices


Course Learning Outcomes:
The student will be able to
1. Understand the fundamentals, advantages and advances in optical communication and integrated photonic devices and circuits.
2. Introduce optical waveguides, detectors, amplifiers, silicon photonics and MEMS applications in photonics.
3. Design, operate, classify and analyze Semiconductor Lasers, LEDs, modulators and other Integrated photonic devices.
4. Identify, formulate and solve engineering-technological problems related optoelectronic integration.
Recommended Books:


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</table>
Course Objectives: In this course the students will learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits.


Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.


Radiation Effects in semiconductor memories.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about Basics of memory chip Design and Technology.
2. Acquire knowledge about RAM and DRAM Design.
4. Work using Laplace Trans., CTFT and DTFT.
5. Acquire knowledge about High-Performance Subsystem Memories

Recommended Books:

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Course Objectives: In this course the students will learn basics of comparator circuits, data converters, implementation of A/D and D/A converters and their performance analysis with design challenges.


Data Converters: Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL.

High Speed A/D Converter Architectures: Flash, Folding, Interpolating, pipelined

High Speed D/A Converter Architectures: Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converters.

Design of multi channel low level and high level data acquisition systems using ADC/DAC, SHA and Analog multiplexers, Designing of low power circuits for transducers.

Sigma-Delta Data Converter Architectures: Programmable Capacitor Arrays (PCA), Switched Capacitor converters, Noise Spectrum, Sigma-Delta Modulation Method, Sigma-Delta A/D and D/A Converters, Non Idealities.

Key Analog Circuit Design: Analog VLSI building blocks, Operational Amplifiers for converters, advanced op-amp design techniques, Voltage Comparators, Sample-and-Hold Circuits.


Course Learning Outcomes:
The student will be able to
1. Apply knowledge of mathematics, science, and engineering to design CMOS analog circuits to achieve performance specifications.
2. Identify, formulates, and solves engineering problems in the area of mixed-signal design.
3. Use the techniques and skills for design and analysis of CMOS based switched capacitor circuits.
4. Work as a team to design, implement, and document a mixed-signal integrated circuit.
Recommended Books:

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Course Objectives: In this course the students will learn the basics of VLSI design for high speed processing, methods for logical efforts, logic styles, latching strategies, interface techniques and related issues.

Introduction of High Speed VLSI Circuits Design

Back-End-Of-Line Variability Considerations: Ideal and non ideal interconnect issues, Dielectric Thickness and Permittivity

The Method of Logical Effort: Delay in a logic gate, Multi-stage logic networks, Choosing the best number of stages.

Deriving the Method of Logical Effort: Model of a logic, Delay in a logic gate, Minimizing delay along a path, Choosing the length of a path, Using the wrong number of stages, Using the wrong gate size.


Circuit Design Margining: Process Induced Variations, Design Induced Variations, Application Induced Variations, Noise

Latching Strategies: Basic Latch Design, Latching single-ended logic, Latching Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques


Clocking Styles: Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

Skew Tolerant Design.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about High Speed VLSI Circuits Design.
2. Identify the basic Back-End-Of-Line Variability Considerations.
3. Understand the Method of Logical Effort.
4. Understand the Circuit Design Margining and Latching Strategies.
5. Understand the Clocking Styles.
Recommended Books:


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Course Objectives: In this course the students will the basics of fault and error models in VLSI arithmetic, fault tolerance strategies, detection and correction techniques and applications of arithmetic units and systems.

Motivation of fault tolerance in arithmetic systems, Fault and error models in VLSI arithmetic units, Reliability and fault tolerance definitions, Reliability and availability modeling.

Estimation of the reliability and availability of fault tolerant systems, Fault diagnosis, Fault tolerance measurement.

Fault tolerance strategies: detection, correction, localization, reconfiguration, Error recovery, Error detecting and correcting codes.

Detection/correction techniques: modular redundancy, time redundancy (e.g., RESO, RERO, REDWC, RETWV, REXO), datacoding (e.g., AN codes, residue codes, GAN codes, RBR codes, Berger codes, residue number systems), algorithm-based techniques, Reconfiguration techniques.

Applications to arithmetic units and systems (e.g., convolvers, inner product units, FFT units neural networks), Application levels: unit, processing element, subsystem, system. Cost/benefit analysis Fault-tolerant transaction processing systems; Fault-tolerant Networks; Redundant disks (RAID).

Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery.

Architecture and design of fault – tolerant computer systems using protective redundancy.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about fault tolerance in arithmetic circuits.
2. Learn about Fault diagnosis, Fault tolerance measurement.
3. Acquire knowledge about Fault tolerance strategies.
4. Enhance capabilities about applications of fault tolerant designs in arithmetic units and systems.
5. Acquire knowledge on Software reliability models, and methods.

Recommended Books:

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</table>
Course Objectives: In this course the students will learn basic concept of MEMS devices, their working principles, equivalent circuits, different MEMS sensors, fabrication technologies, modeling and characterization tools and calibration techniques.

Introduction to MEMS: Introduction to MEMS and Micro sensors, MEMS system-level design methodology, Equivalent Circuit representation of MEMS, Signal Conditioning Circuits.

Principles of Physical and Chemical Sensors: Sensor classification, Sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.

Sensor Technology: Concept of clean room, Vacuum systems, Thin Film Materials and processes (Lithography, oxidation, sputtering, diffusion, CVD, micro machining, Wafer bonding, Wire bonding and Packaging.

Sensor Modeling: Numerical modeling techniques, Model equations, different effects on modelling (mechanical, electrical, thermal, magnetic, optical, chemical and biological and example of modelling.

Sensor characterization and Calibration: Basic measurement and characterization systems, study of static and dynamic Characteristics, Sensor reliability, Ageing Test, failure mechanism.

Sensor Applications: Pressure Sensor with embedded electronics, Accelerometer, RF MEMS Switch with electronics, Bio-MEMS, environmental monitoring (Gas Sensors).

Future Aspects of MEMS: NEMS, MOEMS, BIO-MEMS, RF MEMS, OPTICAL MEMS.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about MEMS & Micro Sensors.
2. Understand various micro fabrication technologies.
3. Gather knowledge of characterization tools.
4. Acquire knowledge about Device Applications

Recommended Books:
### Evaluation Scheme:

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Course Objectives: In this course the students will learn VLSI Cad tools and its related concepts, algorithms, Design automation of FPGA and high level synthesis.

Introduction to VLSI Design: Automation, use of VLSI CAD tools, Algorithmic Graph Theory, Computational Complexity and ROBDD; Partitioning and Placement: KL algorithm, FM algorithm, Group-migration algorithm, Simulated Annealing and Evolution

Floor planning and Pin Assignment, Placement, Layout styles, Discrete methods in global placement, Timing-driven placement, Routing: Global Routing, detailed routing, Graph models, Line Search, Maze Routing, Channel Routing, Steiner Tree based Algorithms, ILP base approaches

Performance Issues in circuit layout: delay models, timing driven placements, timing driven routing, Via Minimization, Over the Cell Routing – Single layer and Two layer routing, Clock and Power Routing

Compaction : Problem formulation, One Dimension compaction, Two Dimension compaction, Hierarchical Compaction, Compaction Algorithms. Physical Design Automation in FPGAs

High level synthesis: Introduction to HDL, HDL to DFG, operation scheduling: constrained and unconstrained scheduling, ASAP, ALAP, List scheduling, Force directed Scheduling, operator binding, Static Timing ANalyss: Delay models, setup time, hold time, cyvcle time, critical paths, Topological mvs. Logical timing analuysis, False paths, Arrival time (AT), Required arrival Time (RAT), Slacks.

Course Learning Outcomes:
The student will be able to
1. Understand of VLSI Design Automation.
2. Acquire knowledge about CAD tools used for VLSI design.
3. Able to understanding Algorithms for VLSI Design Automation.
4. Able to gather knowledge of High Level Synthesis.
5. Understand Timing Analysis

Recommended Books:
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Course Objectives: In this course the students will learn the basic fundamental of OTA architecture, amplifiers, voltage followers, floating gate circuits along with its applications, switched capacitor techniques and implementations.

Review of basic Op Amps and OTA Architectures, Conventional Op Amps, OP Amp Limitations, 3 dB time constant computation.

Nested and Reversed Gm-C Op Amplifiers. Recent settling time techniques, Enhanced Gm-C Amp for Large capacitive load.

Line Driver Amplifiers, Band gap and references, Low voltage cells, Low Voltage current source implementation,

Flipped voltage follower and applications, Rail-to-rail amplifiers, Fully balanced fully symmetric circuits.

Bulk-driven circuits, Floating Gate circuits and its applications.

LDO Fundamentals, Class D amplifiers, Multipliers: Power, linearity and area tradeoffs

P-N Rail to Rail Stages and Low Voltage Cells, Voltage References

Common-Mode Feedback & Feedforward: Theory and Practice, Non-linearity issues and Noise Considerations

Linearized OTA and Fully-Differential OTA: CMFB control techniques. Negative resistors and capacitors.

Low Voltage Switched-Capacitor Techniques, Comparators & Sample and Hold circuits

Negative Capacitor and Resistor Implementations

Course Learning Outcomes:
The student will be able to
1. Apply knowledge of mathematics, science, and engineering to design and analysis of modern analog integrated circuits.
2. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.
3. Understand the relationships between devices, circuits and systems.
4. Participate and function within multi-disciplinary teams.

Recommended Books:
Selected copies of Journal Papers and notes.

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Course Objectives: In this course the students will learn SOC design processes, ASIC design flow, EDA tools, architecture design and test optimization with system integration issues.

Overview of SOC Design Process: Introduction, Top-down SoC design flow, Metrics of SoC design, Techniques to improve a specific design metric, ASIC Design flow and EDA tools.


SOC Design and Test Optimization: Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition.

Course Learning Outcomes:
The student will be able to
1. Acquire knowledge about Top-down SoC design flow.
2. Understand the ASIC Design flow and EDA tools.
3. Acquire knowledge about Front-end and back-end chip design.
4. Understand the designing communication Networks.
5. Understand the design space exploration.
6. Understand the design methodologies for SoC

Recommended Books:

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Course Objectives: In this course the students will learn redundant number systems, algorithms for fast addition, VLSI implementation aspects, High speed multiplication, VLSI layout considerations, algorithms for fast division and impact of hardware technology.

Numbers and Arithmetic: Review of Number systems, their encoding and basic arithmetic operations, Class of Fixed-Radix Number Systems, Unconventional fixed-point number systems, Representing Signed Numbers, Negative-radix number Systems, Redundant number Systems, Residue Number Systems.


High-Speed Multiplication: Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers, VLSI layout considerations.

Fast Division and Division Through Multiplication: Basic Division Schemes, Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Division by Convergence, Hardware implementation.


Course Learning Outcomes:
The student will be able to
1. Understand power fundamentals: design objective, quantification of energy and power.
2. Work with fast adders.
3. Analyze the issues related to trade-off between cost, speed and accuracy.
4. Work with high throughput, low power algorithms.

**Recommended Books:**


**Evaluation Scheme:**

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<tr>
<th>S.No.</th>
<th>Evaluation Elements</th>
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<td>3.</td>
<td>Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)</td>
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