UEI844 VLSI DESIGN FOR TESTABILITY

L	T	P	Cr
3	1	0	3.5

Introduction to VLSI testing: Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing, Types of Testing, Automatic Test Equipment, Electrical Parametric Testing

Test economics and product quality: Defining Costs, Benefit-Cost Analysis, Economics of Testable Design, Yield, Defect Level as a Quality Measure, Test Data Analysis, Defect Level Estimation

Fault modeling: Defects, Errors, and Faults, Levels of Fault Models, Single Stuck-at Fault, Fault Equivalence, Fault Collapsing, Fault Dominance and Checkpoint Theorem

Logic and fault simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation, Algorithms for Fault Simulation, Statistical Methods for Fault Simulation

Combinational circuit test generation: Algorithms and Representations, Redundancy Identification, Automatic Test-Pattern Generator (ATPG), Combinational ATPG Algorithms, Test Generation Systems, Test Compaction

Sequential circuit test generation: ATPG for Single-Clock Synchronous Circuits, ATPG for Single-Clock Synchronous Circuits, Approximate Methods, Cycle-Free Circuits, Cyclic Circuits

Text Books:

1. *Bushnell, M.L. and Agrawal, V. D., Essentials of electronic testing for digital memory and mixed signal VLSI circuits, Kluwer Academic Publishers (2002).*

Reference Books:

1. *Abramovici, M. and Friedman, A. D., Digital Systems Testing and Testable Design, Jaico Publishing House (2001).*

Evaluation Scheme:

Sr. No.	Evaluation Elements	Weightage (%)
1	MST	30
2	EST	45
3	Sessionals (May include Assignments/Projects/Tutorials/Quizzes/Lab Evaluations)	25