Course Syllabi: UEI301 Digital Electronics (L : T : P :: 3 : 1 : 2)

1. **Course number and name:** UEI301; Digital Electronics

2. **Credits and contact hours:** Credits: 4.5; Hours: 6

3. **Text book, title, author, and year**

   - *Floyd, T.L. and Jain, R. P., Digital Fundamentals, Pearson Education (2008) 10th ed.*
   - *Tocci, R. and Widmer, N., Digital Systems: Principles and Applications, Pearson Education (2007) 10th ed.*
   - *Mano, M. M. and Ciletti, M., Digital Design, Pearson Education (2008) 4th ed.*
   - *Kumar, A., Fundamentals of Digital Circuits, Prentice Hall (2007) 2nd ed.*

   a. Other supplemental materials
      - Nil

4. **Specific course information**

   a. Brief description of the content of the course (catalog description)

   Introduction: Difference between analog and digital systems, Advantages and Disadvantages of digital system.

   Number Systems: Introduction, Number systems: Decimal, Binary, Octal, Hexadecimal; Conversions; Representation of Signed Numbers, Sign magnitude, 1's complement, 2's complement, r's complement; Binary Arithmetic – addition, subtraction, multiplication and division, Binary codes: Weighted and non-weighted codes, Sequential codes, Self-complementing codes, Excess-3 code, Gray code, Error-detecting codes, Error-correcting codes, Hamming code, Alphanumeric codes.

   Minimization Techniques: Introduction, Boolean Algebra: Laws and Theorems, Demorgan's Theorem, Simplification of Boolean functions by Boolean algebra, K-map method and Quine-McClusky method in SOP and POS forms, Advantages and disadvantages of different minimization techniques.

   Combinational Circuits: Introduction, Logic Gates: Basic gates, Universal gates, Derivation of other gates from universal gates, Half adder, Full adder, Parallel Binary adder, Serial adder, BCD adder, Half and Full subtractor, Binary multiplier, Dividers, ALU, Code converters, Magnitude comparators, Parity Generators/checkers, Encoders, Priority encoder, Decoders, Multiplexers, Multiplexer as function generator, Demultiplexer.

   Sequential Circuits: Introduction, Flip-flops: Types, their conversions and applications, Registers: Serial/Parallel in/out, Bi-directional, Universal shift register, Counters: Synchronous, Asynchronous, Decade, Binary, Modulo-n, Shift register counters; Design of Synchronous sequential circuits.

   Memories: Introduction and classification of ROM, ROM organization, Static and Dynamic RAM, DRAM Refreshing, Representative circuits for cells using BJT and FET's, Timing diagrams of memories, Memory expansion using IC's, Flash memory, CCD, Magnetic Memories.

   Logic circuits: Introduction, Specification terminology: Fan out, Unit load, Current and voltage parameters; TTL, ECL, MOS, CMOS logic families and their comparison, Tristate Logic, Interfacing of TTL and CMOS logic families.

Converters: Digital to Analog conversion, R-2R ladder DAC, Weighted Resistor DAC, Analog-to-Digital (A/D or ADC) conversion, Flash type, Counter type ADC, Dual-slope ADC, Successive approximation type ADC.

Laboratory work

To consider various important codes and the logic for converting from one to another, 74146, 7476, 7483, 7485, 7490, 7492, 7495, 74121, 74123, 74126, 74151, 74163, 74180, 74181, 74190, 74192, 74195, 74196, Shift register and binary counting using JK flip flop, asynchronous/synchronous up/down counters, Variable modulus counters, Usage of IC tester, Computer simulation using EDA tools.

5. **Specific goals for the course**

After the completion of the course, the students will be able to:

- Describe the number systems, conversions and their applications.
- Apply minimization techniques such as K maps, Tabular method etc for the design of digital circuits.
- Design combinational and sequential circuits.
- Differentiate various type of memories and there use in different applications.
- Demonstrate the concept of logic circuits and converters.

6. **Brief list of topics to be covered**

- Number System
- Minimization techniques
- Combinational and Sequential Circuits
- Memory
- Logic Circuit and Converters