PVL FPGA BASED SYSTEM DESIGN

L	T	P	Cr
3	0	2	4.0

requisite: Digital Electronics

roduction: Concepts of Hardware Description Languages and logic synthesis. (2L)

c synthesis: Design cycle, types of synthesizers, design testing and verification, design optimization techniques, technology mappi DL design hierarchy, objects, types and subtypes, design organization, VHDL design cycle. (5L)

ombinational Logic: Design units, entities and architectures, simulation and synthesis model, signals and ports, simple signal assignm conditional signal and ents, selected signal assignment. (5L)

ypes and Operators: Synthesizable types, standard types, standard operators, scalar types, records, arrays, attributes, standard opera ator precedence, Boolean operators, comparison operators, arithmetic operators, concatenation operators. (5L)

ackage std_logic_arith: std_logic_arith package, making the package visible, content s of std_logic_arith, resize functions, operators, tions, type conversions, constant values, mixing types in expressions, numeric packages. (3L)

Sequential VHDL: Processes, signal assignments, variables, if statements, case statements. (3L)

sters: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers, simulation model nchronous reset, asynchronous reset templates, registered variables. (3L)

archy: Role of components, using components, component instances, component declaration, Configuration specifications, default bind ing process, component packages, generate statements. (4L)

b programs: Functions, type conversions, procedures, declaring subprograms. (3L)

Benches: Test benches, verifying responses, clocks and resets, printing response values, ing data files, reading standard types, error handling. (3L)

braries: Standard libraries, organising files, library names, library work, incremental compilation. (2L)

SM: Moore and Mealy machine modelling (3L)

GA: Introduction, Logic Block Architecture, Routing Architecture, Programmable, Interconnection, Design Flow, Xilinx Virt chitecture), Boundary Scan, Programming FPGA's, Constraint Editor, Static Timing Analysis, One hot encoding, Applications, Tools, Study, Xilinx Virtex II Pro.. (4L)

aboratory Work: Modeling and simulation of all VHDL constructs using ModelSim, their testing by modeling andsimulating test benche c Synthesis using FPGA Advantage, Mapping on FPGA Boards. (15)

XT BOOKS

ERENCE BOOKS

1. Charles H. Roth, Digital System Design Using VHDL , Jr.,Thomson, (2008)2nd Ed.
2. Bhaskar, J., A VHDL Primer, Pearson Education/ Prentice Hall (2006)3rd Ed.

1. Rushton, A., VHDL for Logic Synthesis, Wiley (1998) 2ed.
2. Ashenden, P., The Designer's Guide To VHDL, Elsevier (2008) 3rd ed.