# SCHEME OF COURSES FOR
MTech (VLSI Design and CAD)

## First Semester

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Course No.</th>
<th>Course Name</th>
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<th>P</th>
<th>Cr</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>PVL101</td>
<td>Physics of Semiconductor Devices</td>
<td>3</td>
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<td>2.</td>
<td>PVL102</td>
<td>IC Fabrication Technology</td>
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<td>3.</td>
<td>PVL103</td>
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<td>4.</td>
<td>PVL104</td>
<td>CAD Systems Environment</td>
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<td>5.</td>
<td>PVL105</td>
<td>Logic Synthesis using HDLs</td>
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## Second Semester

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<tbody>
<tr>
<td>1.</td>
<td>PVL201</td>
<td>Analog IC Design</td>
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<td>2.</td>
<td>PVL202</td>
<td>Embedded Systems</td>
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<td>3.</td>
<td>PVL203</td>
<td>VLSI Signal Processing</td>
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## Third Semester

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<tr>
<td>1.</td>
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## Fourth Semester

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<td>PVL091</td>
<td>Thesis (Contd …)</td>
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Total Credits – 50

Approved by the Senate in its 70th meeting held on May 25,2009
List of Electives

Elective–I

<table>
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<tr>
<th>S. No.</th>
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<td>1.</td>
<td>PVL211</td>
<td>VLSI Architectures</td>
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<td>PEC212</td>
<td>Audio and Speech Processing</td>
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Elective–II

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<tr>
<td>1.</td>
<td>PVL221</td>
<td>VLSI Subsystem Design</td>
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<td>PVL222</td>
<td>ASICs and FPGAs</td>
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<td>PVL223</td>
<td>VLSI Testing and Verification</td>
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<td>PVL224</td>
<td>MOS Device Modeling</td>
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<td>PCS203</td>
<td>Soft Computing</td>
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<td>PEC202</td>
<td>Advanced Wireless Communication Systems</td>
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Electives–III

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<tr>
<td>1.</td>
<td>PVL331</td>
<td>Memory Design and Testing</td>
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<td>PVL333</td>
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<td>PVL334</td>
<td>High Speed VLSI Design</td>
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<td>PVL335</td>
<td>Fault Tolerance in VLSI</td>
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Electives–IV

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<tr>
<td>1.</td>
<td>PVL341</td>
<td>Low Power Design Techniques</td>
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<td>Hardware Algorithms for Computer Arithmetic</td>
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<td>Optical VLSI</td>
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<td>PEC322</td>
<td>Video and Image Processing</td>
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Prerequisite(s): None

Semiconductor Electronics: Physics of Semiconductor Materials, Drift Velocity, Mobility, Scattering, Diffusion current Band Model.

Metal Semiconductor Contacts: Metal-Semiconductor System, (V-I) and (C-V) Equations for a Shottky - Barrier - Diode, Diode Construction, Device Analysis using Surface States, Applications as Mixer and Detectors in Microwave Region, Ohmic Contacts, Surface Effects.


Recommended Books
PVL102 IC FABRICATION TECHNOLOGY

Prerequisite(s): None

Crystal Growth and Wafer Preparation: Electronic Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Processing Considerations.


Etching: Reactive plasma etching, AC and DC plasma excitation, plasma properties, chemistry and surface interactions, feature size control and an isotropic etching, ion enhanced and induced etching, properties of etch processes. Reactive - Ion - Beam – Etching, Specific etch processes: PolySi/Polycide, Trench etching, SiO2 and Si3N4.

Sub-micron Process Techniques; ULSI Technology; Nano-Fabrication.

Recommended Books

Prerequisite(s): None


Static CMOS Logic Elements: Complex Logic Functions, CMOS NAND Gate, CMOS NOR Gate, Complex Logic Gates, Exclusive OR and Equivalence Gates, Adder Circuits, Pseudo-nMOS Logic Gates, Schmitt Trigger Circuits, SR and D-type Latch, CMOS SRAM Cell, Tri-state Output Circuits.


Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families: Charge Leakage, Charge Sharing, Dynamic RAM Cell, Bootstrapping, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Multiple-Output Domino Logic, NOR Logic, Single-Phase Logic.

Effects of Technology Scaling on CMOS Logic Styles: Trends and Limitations of CMOS Technology Scaling – MOSFET Scaling Trends, Challenges of MOSFET Scaling – Short-Channel Effects, Subthreshold Leakage Currents, Dielectric Breakdown, Hot Carrier effects, Soft Errors, Velocity Saturation and Mobility Degradation, DIBL, Scaling down V_{dd}/V_{th} ratio.

CMOS Differential Logic Styles: Dual-Rail Logic, CVSL, CPL, DPL, DCVS, MCML.


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**Laboratory Work**

Familiarization with schematic and layout entry using Mentor/ Cadence/ Tanner Tools, circuit simulation using SPICE; DC transfer Characteristics of Inverters, Transient response, Calculating propagation delays, rise and fall times, Circuit design of inverters, complex gates with given constraints; Circuit Simulation and Performance Estimation using SPICE; Layouts of Inverters and Complex gates, Layout Optimization, Design Rule Check (DRC), Electrical Rule Check (ERC), Comparison of Layout Vs. Schematics, Circuit Extraction.

**Recommended Books**

PVL104 CAD SYSTEMS ENVIRONMENT

Prerequisite(s): None

Introduction: Familiarity with UNIX/LINUX operating systems.

Operating System: Basic Concept of Operating System: Evolution of operating system, fundamental of operating system functions, multiprogramming, multiprocessing, time sharing systems and real time systems.

Linux: About Linux, Brief History, Linux, Distributions, Using the Emacs Editor, Using the vi Editor, Using the Pico Editor, Introduction to Users and Groups Essentials of Effective User, Group, and Password Management, Introduction to the Linux Kernel, Using Kernel Modules, Compiling the Linux Kernel, Installing the Linux Kernel, File System, Disk Geometry.

Shell Programming: Familiarity with different shells, UNIX Utilities like tar, make, yacc, lex, lint, debugger etc.

Scripting Languages: Brief Introduction and overview of Perl, Tcl/tk.


Laboratory Work
UNIX/LINUX - Familiarity with different shells, UNIX/LINUX Utilities like tar, make, lex, lint, etc. Exercises of Perl and Tcl/tk, File Formats - .tgz, .tar; Programming exercises using SystemC.

Recommended Books

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PVL105 LOGIC SYNTHESIS USING HDLS

Prerequisite(s): None

Introduction: Concepts of Hardware Description Languages and logic synthesis.

Logic synthesis: Design cycle, types of synthesizers, design testing and verification, design optimization techniques, technology mapping, VHDL design hierarchy, objects, types and subtypes, design organization, VHDL design cycle.

RTL Level Design: RTL design stages, VHDL description of the RTL design.

Combinational Logic: Design units, entities and architectures, simulation and synthesis model, signals and ports, simple signal assignments, conditional signal assignments, selected signal assignment.

Types: Synthesizable types, standard types, standard operators, scalar types, records, arrays, attributes.

Operators: standard operators, operator precedence, Boolean operators, comparison operators, arithmetic operators, concatenation operators.

Package std_logic_arith: std_logic_arith package, making the package visible, contents of std_logic_arith, resize functions, operators, shift functions, type conversions, constant values, mixing types in expressions, numeric packages.

Sequential VHDL: Processes, signal assignments, variables, if statements, case statements.

Registers: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers, simulation model of asynchronous reset, asynchronous reset templates, registered variables.

Hierarchy: Role of components, using components, component instances, component declaration, Configuration specifications, default binding, binding process, component packages, generate statements.

Sub programs: Functions, type conversions, procedures, declaring subprograms.

Test Benches: Test benches, verifying responses, clocks and resets, printing response values, reading data files, reading standard types, error handling.

Libraries: Standard libraries, organising files, library names, library work, incremental compilation.

Basic principles of Combinational logic design, sequential logic design, arithmetic circuit design and control logic design.
Laboratory Work
Modeling and simulation of all VHDL constructs using ModelSim, their testing by modeling and simulating test benches, Logic Synthesis using FPGA Advantage, Mapping on FPGA Boards.

Recommended Books
PVL201 ANALOG IC DESIGN

Prerequisite(s): None


Single Stage Amplifiers: Common Source Stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode.

Differential Amplifier: Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell.

Current Sources and Mirrors: Current Sources, Basic Current Mirrors, Cascode Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis.

Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.

Voltage References: Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References.

Feedback: General Considerations, Topologies, Effect of Loading.

Operational Amplifier: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR.

Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques.

Noise: Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

Switched-Capacitor Circuits: Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.


Laboratory Work
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Review of Mentor Tools; Analysis of Various Analog Building Blocks such as, Current and Voltage References/Sources, Current Mirrors, Differential Amplifier, Output Stages; Design and Analysis of Op-Amp (Closed loop and open loop) and its Characterization, Switched-Capacitor Integrator; Analog Layout Constraints, Layout Designs and Analysis.

**Recommended Books**

PVL202 EMBEDDED SYSTEMS

L T P Cr
3 0 2 4.0

Prerequisite(s): None

**Embedded Processing:** Introduction to Embedded Computing, Difference between Embedded and General-Purpose Computing, Characterizing Embedded Computing, Design Philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, Role of the Compiler, Architectural structures, The datapath, Registers and Clusters, Memory Architecture, Branch architecture, Speculation and prediction, Prediction in the embedded domain, Register File Design, Pipeline Design, the control unit, control registers.

**Embedded Processors:** Microprocessor versus Microcontroller architecture, ARM architecture, Embedded Cores, Soft and Hard Cores, Architecture of Configurable Microblaze soft core, Instruction set, Stacks and Subroutines, Microblaze Assembly Programming, Input-Output interfacing, GPIO, LCD interfacing, Peripherals, DDR Memory, SDRAM, Microblaze interrupts, Timers, Exceptions, Bus Interfacing, DMA, On-chip Peripheral bus (OPB), OPB Arbitration, OPB DMA.

**RTOS and Application design:** Programming language choices, Traditional C and ANSI C, C++ and Embedded C++, matlab, Embedded JAVA, Embedded C extensions, Real time operating systems, Embedded RTOS, Real time process scheduling, structure of real time operating system, Memory management in Embedded operating system, operating system overhead, interprocess communication mechanisms, File systems in Embedded devices, Different types of locks, Semaphores, Application studies with Vxworks, Montavista Linux etc.

**System Design and Simulation:** System-on-a-Chip (SoC), IP Blocks and Design Reuse, Processor Cores and SoC, Non-programmable accelerators, reconfigurable logic, multiprocessors on a chip, symmetric multiprocessing, heterogeneous multiprocessing, use of simulators, Compilers, Loaders, Linkers, locators, assemblers, Libraries, post run optimizer, debuggers, profiling techniques, binary utilities, linker script, system simulation, In Circuit Emulation, Validation and verification, Hardware Software partitioning, Co-design.

**Laboratory Work**
Embedded System design using Embedded Development Kit Software and implementation on FPGA hardware, Practicals on Xilkernel, Vxworks and montavista Linux Real Time Operating Platforms.

**Recommended Books**

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PVL203 VLSI SIGNAL PROCESSING

Prerequisite(s): None

Introduction: Introduction to DSP Systems, Terminating and Non-Terminating, Representation of DSP programs, Data Flow graphs (DFGs), Single rate and multi rate DFGs, Iteration bound, Loop, Loop Bound, Iteration rate, Critical loop, Critical path, Area-Speed-Power trade-offs, Precedence constraints, Acyclic Precedence graph, Longest Path Matrix (LPM) and Minimum Cycle Mean (MCM) Algorithms, Pipelining and parallel processing of DSP Systems, Low Power Consumption.

Algorithmic Transformations: Retiming, Cut-set retiming, Feed-Forward and Feed-Backward, Clock period minimization, register minimization, Unfolding, Sample period reduction, Parallel processing, Bit-serial, Digit-serial and Parallel Architectures of DSP Systems, Folding, Folding order, Folding Factor, Folding Bi-quad filters, Retiming for folding, Register Minimization technique, Forward Backward Register Allocation technique.

Systolic Architecture Design and Fast Convolution: Systolic architecture design methodology, Projection vector, Processor Space vector, Scheduling vector, Hardware Utilization efficiency, Edge mapping, Design examples of systolic architectures, Cook-Toom Algorithm and Modified Cook-Toom Algorithm, Wniorad Algorithm and Modified Winograd Algorithm, Iterated Convolution, Cyclic Convolution.


Recommended Books:
PVL211 VLSI ARCHITECTURES

Prerequisite(s): None

**Complex Instruction Set Computers (CISC):** Instruction Set, Characteristics and Functions, Addressing Modes, Instruction Formats, Architectural Overview, Processor Organization, Register Organization, Instruction Cycle, Instruction Pipelining, Pentium Processor, PowerPC Processor.

**Reduced Instruction Set Computers (RISC):** Instruction execution Characteristics, Register Organization, Reduced Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview, RISC Pipelining, Motorola 88510, MIPS R4650, RISC Vs. CISC.

**Pipeline Processing:** Basic Concepts, Classification of Pipeline Processors, Instruction and Arithmetic Pipelining: Design of Pipelined Instruction Units, Pipelining Hazards and Scheduling, Principles of Designing Pipelined Processors.

**Memory Architectures:** Memory hierarchy design, Multiprocessors, thread level parallelism and multi-core architectures, I/O buses. Arithmetic: Fixed point, Floating point and residue arithmetic, Multiply and Divide Algorithms.
Issues in arithmetic system design, Issues in the applications (optimizing the hardware – software interface), ASIP, reconfigurable computing, Future microprocessor architectures.

**Superscaler Processors:** Overview, Design Issues, PowerPC, Pentium.

**Recommended Books**

PVL212 PHYSICAL DESIGN AUTOMATION

Prerequisite(s): None

Introduction to VLSI Physical Design Automation, use of VLSI CAD tools, Algorithmic Graph Theory, computational Complexity and ROBDD; Partitioning and placement: KL algorithm, FM algorithm etc.


Performance issues in circuit layout, delay models, timing driven placement, timing driven routing, Via Minimization, Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.

Compaction, compaction algorithms, Physical Design Automation of FPGAs.

High Level Synthesis: Introduction to HDL, HDL to DFG, operation scheduling: constrained and unconstrained scheduling, ASAP, ALAP, List scheduling, Force directed scheduling, operator binding; Static Timing Analysis: Delay models, setup time, hold time, cycle time, critical paths, Topological vs. logical timing analysis, False paths, Arrival time (AT), Required arrival Time (RAT), Slacks.

Recommended Books

PVL213 NANO-ELECTRONICS

L T P Cr
3 0 0 3.0

Prerequisite(s): None

Shrink-down approaches: Introduction to Nanoscale Systems, Length energy and time scales, Top down approach to Nanolithography, CMOS Scaling, Limits to Scaling, System Integration Limits - Interconnect issues, etc.

Overview of Nanoelectronics and Devices: The Nano-scale MOSFET, FinFETs, Vertical MOSFETs, Resonant Tunneling Transistors, Single Electron Transistors, New Storage devices, Optoelectronic and Spin electronics Devices.

Basics of Quantum Mechanics: History of Quantum Mechanics, Schrödinger Equation, Quantum confinement of electrons in semiconductor nano structures, 2D confinement (Quantum Wells), Density of States, Ballistic Electron Transport, Coulomb Blockade, NEGF Formalism, Scattering.


Future Aspects of Nanoelectronics: Molecular Electronics: Molecular Semiconductors and Metals, Electronic conduction in molecules, Molecular Logic Gates, Quantum point contacts, Quantum dots and Bottom up approach, Carbon Nano-tube and its applications, Quantum Computation and DNA Computation.

Overview of Organic Electronics: OLEDs, OLETs, Organic Solar Cells.

Recommended Books

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PVL214 PROCESS AND DEVICE CHARACTERIZATION

Prerequisite(s): None

Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometry, FTIR.


Material and Impurity Characterization: SIMS, XRD, EDAX.


Process and SPICE model parameter Extraction: SPICE BSIM3 model parameter extraction and optimization, Intrinsic Most and extrinsic, parasitic element, EKV model, Gummel-Poon model, BSIM model.

Test Structures for Process Characterization: Contact Resistors, Split Cross Bridge Resistors, Self-aligned n+ Bridges.

Test Structures for Device Characterization: Individual MOSFETs, 4x4 MOSFET Arrays, Capacitors.

Test Structures for Faults and Reliability Analysis: Contact Chains, Serpentine/Comb Resistors.

Recommended Books
PVL345 REAL TIME SOFTWARE AND SYSTEMS

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Prerequisite(s): Exposure to PVL104 CAD System Environment


**Real-Time Scheduling and Schedulability Analysis:** Clock-driven scheduling, Priority-driven scheduling of periodic tasks, Scheduling a periodic and sporadic jobs in priority-driven systems, Function Queue Scheduling and Date Shard and Reentrancy.

**Embedded Software**
Examples of embedded system, Characteristic and Typical Hardware Components, Embedded Software Architectures, Round Robin, and Interrupts, Memory Architecture and Devices, Memory Interface.


**Recommended Books**
PVL221 VLSI SUBSYSTEM DESIGN

Prerequisite(s): Exposure to PVL103 Digital VLSI Design


VLSI Design Flow, Design Methodologies, Abstraction Levels.


Design of Control Part: Moore and Mealy Machines, PLA Based Implementation, Random Logic Implementation, Micro-programmed Implementation.


Memory Design: SRAM cell, Various DRAM cells, RAM Architectures, Address Decoding, Read/Write Circuitry, Sense Amplifier and their Design, ROM Design.

Clocking Issues: Clocking Strategies, Clock Skew, Clock Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree.

Synchronization Failure and Meta-stability.

Laboratory Work
Review of schematic and layout tools using Cadence Univ. tools, circuit design and simulation using SPICE. Use of Design Rule Check (DRC), Electrical Rule Check (ERC), Comparison of Layout Vs. Schematic, Schematic and Layouts design of Sub-system blocks, their characterization, and optimization.

Recommended Books
PVL222 ASICS AND FPGAS

Prerequisite(s): None

Overview: Digital system design options and tradeoffs, Design methodology and technology overview, High Level System Architecture and Specification: Behavioral modeling and simulation.

Review HDLs: Hardware description languages, combinational and sequential design, state machine design, synthesis issues, test benches.

FPGA Architectures And Technologies: FPGA Architectural options, granularity of function and wiring resources, coarse vs. fine grained, vendor specific issues (emphasis on Xilinx).

Logic Block Architecture: FPGA logic cells, timing models, power dissipation.

I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation. Programmable interconnect - Partitioning and Placement, Routing resources, delays.

Applications: Embedded system design using FPGAs, DSP using FPGAs, Dynamic architecture using FPGAs, reconfigurable systems, application case studies.

ASICs: Types of ASICs, ASIC design flow, Programmable ASICs, Anti-fuse, SRAM, EPROM, EEPROM based ASICs, Programmable ASIC logic cells and I/O cells, Programmable interconnects.

ASIC Methodologies (classical) and ASIC Methodologies (aggressive).

Laboratory Work
Simulation/implementation exercises of combinational, sequential and DSP kernels on Xilinx/FPGA boards.

Recommended Books
PVL223 VLSI TESTING AND VERIFICATION

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Prerequisite(s): None

Faults: Physical Faults and their modeling; Stuck-at faults; Bridging Faults; Fault collapsing, Fault Simulation; Deductive, Parallel and Concurrent Fault Simulation; Critical Path Tracing.

ATPG for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM; Random, Exhaustive and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

PLA Testing: Cross Point Fault Model and Test Generation.

Memory Testing: Permanent, Intermittent and Pattern Sensitive Faults; Marching Tests; Delay Faults;

ATPG for Sequential Circuits; Time Frame Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board level Testing; BIST and Totally Self Checking Circuits; System Level diagnosis.

Introduction: Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes; Reconfiguration Techniques; Yield Modeling Reliability and effective area utilization.

Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SoCs.

Verification: Design verification techniques based on simulation, analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Laboratory Work
Logic Simulation, Logic level diagnosis, ATPG, Implementation of BIST for a given module and system level diagnosis using DFT tools.

Recommended Books
PVL224 MOS DEVICE MODELING

Prerequisite(s): Exposure to PVL101 Physics of Semiconductor Devices

Semiconductor Fundamentals: Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations (electron statistics, density of states, effective mass, bandgap narrowing), Review of PN and MS diodes.

Quantum Mechanics Fundamentals: Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling.

Modeling and Simulation of Carrier Transport: Carrier Scattering (impurity, phonon, carrier-carrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion.

MOS Capacitors: Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown).

MOSFET Modeling: Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices.


Advanced Device Technology: SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash).

Sub-micron and Deep sub-micron Device Modeling.

Laboratory Work
SPICE simulations, Study of SPICE Models, Extraction of Model Parameters for various devices in different technologies.

Recommended Books

Approved by the Senate in its 70th meeting held on May 25, 2009
Prerequisite(s): None


Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.


High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.

Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.


Radiation Effects in semiconductor memories.

Recommended Books


PVL332 MIXED SIGNAL CIRCUIT DESIGN

Prerequisite(s): Exposure to PVL-201 Analog IC Design


Data Converters: Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL.


High Speed D/A Converter Architectures: Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converters.

Design of multi channel low level and high level data acquisition systems using ADC/DAC, SHA and Analog multiplexers, Designing of low power circuits for transducers.

Sigma-Delta Data Converter Architectures: Programmable Capacitor Arrays (PCA), Switched Capacitor converters, Noise Spectrum, Sigma-Delta Modulation Method, Sigma-Delta A/D and D/A Converters, Non Idealities.

Key Analog Circuit Design: Analog VLSI building blocks, Operational Amplifiers for converters, advanced op-amp design techniques, Voltage Comparators, Sample-and-Hold Circuits.


Recommended Books


Approved by the Senate in its 70th meeting held on May 25, 2009

Overview of SOC Design Process:
Introduction, Top-down SoC design flow, Metrics of SoC design, Techniques to improve a specific design metric, ASIC Design flow and EDA tools.

SOC Architecture Design:

SOC Design and Test Optimization:
Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition.

Recommended Books
PVL334 HIGH SPEED VLSI DESIGN

Prerequisite(s): None

Introduction of High Speed VLSI Circuits Design.

Back-End-Of-Line Variability Considerations: Ideal and non ideal interconnect issues, Dielectric Thickness and Permittivity.

The Method of Logical Effort: Delay in a logic gate, Multi-stage logic networks, Choosing the best number of stages.

Deriving the Method of Logical Effort: Model of a logic, Delay in a logic gate, Minimizing delay along a path, Choosing the length of a path, Using the wrong number of stages, Using the wrong gate size.

Non-Clocked Logic Styles: Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.


Circuit Design Margining: Process Induced Variations, Design Induced Variations, Application Induced Variations, Noise.


Clocking Styles: Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

Skew Tolerant Design.

Recommended Books

Motivation of fault tolerance in arithmetic systems, Fault and error models in VLSI arithmetic units, Reliability and fault tolerance definitions, Reliability and availability modeling.

Estimation of the reliability and availability of fault tolerant systems, Fault diagnosis, Fault tolerance measurement.

Fault tolerance strategies: detection, correction, localization, reconfiguration, Error recovery, Error detecting and correcting codes.

Detection/correction techniques: modular redundancy, time redundancy (e.g., RESO, RERO, REDWC, RETWV, REXO), datacoding (e.g., AN codes, residue codes, GAN codes, RBR codes, Berger codes, residue number systems), algorithm-based techniques, Reconfiguration techniques.

Applications to arithmetic units and systems (e.g., convolvers, inner product units, FFT units, neural networks), Application levels: unit, processing element, subsystem, system. Cost/benefit analysis Fault-tolerant transaction processing systems; Fault-tolerant Networks; Redundant disks (RAID).

Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery.

Architecture and design of fault – tolerant computer systems using protective redundancy.

**Recommended Books**

PVL341 LOW POWER DESIGN TECHNIQUES

Prerequisite(s): None

Low Power Microelectronics: Retrospect and Prospect, Fundamentals of power dissipation in microelectronic devices, Estimation of power dissipation due to switching, short circuit, sub-threshold leakage, and diode leakage currents.

CMOS Scaling: Scaling for High Performance and Low-Power,

Low Voltage Technologies and Circuits: Threshold Voltage Scaling and Control, Multiple Threshold CMOS (MTCMOS), Substrate Bias Controlled Variable Threshold CMOS, Testing Issues: Design and test of low-voltage CMOS circuits.


Power Conscious High-Level Synthesis.

Silicon-On-Insulator Based Technologies.

Recommended Books

Prerequisite(s): None

**Introduction to RF and Wireless Technology:** Complexity comparison, Design bottleneck, Applications, Analog and Digital systems and choice of technology.

**Basic Concepts in RF Design:** Non linearity and time variance - Effects of non linearity and cascaded nonlinear stages, Inter symbol interference, Random Processes and noise, Sensitivity and dynamic range, Passive Impedance Transformation.

**Modulation and Detection:** General considerations, Analog Modulation: Amplitude modulation, phase and frequency modulation, Digital modulation - basic concepts, binary modulation and quadrature modulation, Power efficiency of modulation schemes - constant and variable envelope signals and spectral regrowth, Noncoherent detection.

**Multiple Access Techniques and Wireless Standards:** Multiple RF communications, Multiple Access Techniques Time and frequency division duplexing, Frequency division multiple access, Time division multiple access and Code division multiple access. Wireless Standards - Advanced mobile phone services, North American Digital Standard, Global system for mobile communication, Qualcomm CDMA and Digital European Cordless Telephone.

**Transceiver Architectures:** General consideration, Receiver Architectures, Heterodyne and Homodyne receivers, Image reject receivers, Digital IF receivers and Subsampling receivers; Transmitter Architectures, Direct conversion transmitters and two step transmitters, Transceiver performance tests.

**Low Noise Amplifiers and Mixers:** Low noise amplifiers - General considerations, Input matching, Bipolar LNAs and CMOS LNAs; Down conversion mixers - General considerations, Bipolar mixers, CMOS mixers and noise in mixers, Cascaded stages.

**Oscillators:** General considerations, Basic LC Oscillator Topologies, Voltage-Controlled Oscillators, Phase Noise - Effect of phase noise in RF communications, Q of an oscillator, Phase noise mechanisms, noise power trade-off, effect of frequency division and multiplication on phase noise, oscillator pulling and pushing, Bipolar and CMOS LC Oscillators, Negative $G_m$ oscillators and interpolative oscillators, Monolithic inductors, Resonator-less VCOs, Quadrature Signal Generations, RC-CR network, Havens technique, frequency division, Single sideband generation.

**Frequency Synthesizers:** General considerations, Phase lock loops - basic concepts, basic PLL, Charge pump PLLs, Types I and II PLLs, noise in PLLs, phase noise at input, phase noise of VCO and frequency multiplication, RF synthesizer architectures, Integer N architecture, fractional N architecture, Dual loop architecture and direct digital synthesis, Frequency dividers divide by two circuits and dual modulus dividers.

**Power Amplifiers:** General considerations, linear and nonlinear PAs, Classification of power amplifiers.
Amplifiers, Class A, B, and C PAs, High efficiency power amplifiers, Large signal impedance matching, Linearization techniques, feedforward, feedback, envelope elimination and restoration and LINC, Design examples.

**Recommended Books**

PVL343 SENSOR TECHNOLOGY AND MEMS

Prerequisite(s): None

Introduction to MEMS: Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Equivalent circuit representation of MEMS, Signal-conditioning circuits and Sensor Noise calculation.

Principles of Physical and Chemical Sensors: Sensor classification, Sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.


Sensor Modeling: Numerical modeling techniques, Model equations, different effects on modeling (mechanical, electrical, thermal, magnetic, optical, chemical and biological) and examples of modeling.


Sensor Applications: Pressure Sensors with embedded electronics, accelerometer with transducer, gyroscope, RF MEMS Switch with electronics, Process engineering, medical diagnostic and patient monitoring, environmental monitoring.

Future Aspects of MEMS: RF MEMS, Optical MEMS, NEMS, MOEMS,

Recommended Books


Approved by the Senate in its 70th meeting held on May 25, 2009
PVL344 HARDWARE ALGORITHMS FOR COMPUTER ARITHMETIC

Prerequisite(s): None

Numbers and Arithmetic: Review of Number systems, their encoding and basic arithmetic operations, Class of Fixed-Radix Number Systems, Unconventional fixed-point number systems, Representing Signed Numbers, Negative-radix number Systems, Redundant Number Systems.


High-Speed Multiplication: Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers, VLSI layout considerations.

Fast Division and Division Through Multiplication: Basic Division Schemes, Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Division by Convergence, Hardware implementation.


Recommended Books

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Introduction: Optical communication: An historical overview, Optical fiber versus copper wire, Integration of Optical communication systems, Optical communication link.

The CMOS Optical Receiver: Simple Resistor Optical Receiver, Transimpedance amplifier, Comparison of transimpedance amplifiers, Multiple-Stages feedback amplifiers, Noise aspects of the transimpedance amplifier, Post amplifier.

Integrated CMOS Optical Receivers: DC-Coupled 0.8\textmu m Digital CMOS 155 Mb/s Optical receiver; 240 Mb/s 18 THz Optical receiver with rail to rail output swing; 1 Gb/s 0.7\textmu m standard CMOS optical receiver; Performance evaluation.

Full Integration of a Standard CMOS Optical Transmitter: LED driver, Integrated CMOS optical fiber link, Integrated CMOS photodiodes, Integrated Photodiodes in sub-micron CMOS.


Recommended Books